

. (

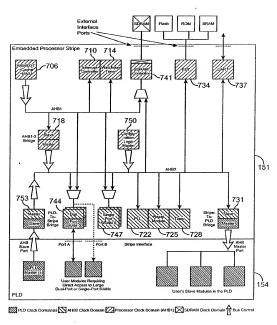


FIG. 7

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FIG. 8

EMBEDDED PROCESSOR STRIPE

FIG. 9

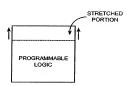
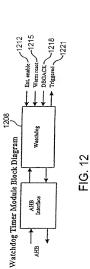


FIG. 10



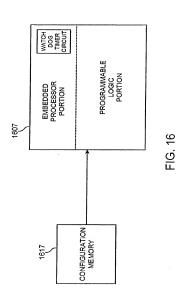
FIG. 11

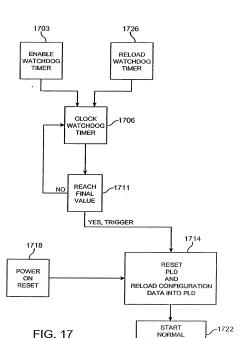


AHB

Address : Address Base + 0x4C0 Control Register (WDOG_CR) - Read/Write Register: WDOG_CR

When this bit has the value 1 further writes to the register have no effect. 0 means watchdog disabled. Other values specify bits 29:4 of the trigger value Access: Read/Write 31 30 39 28 27 36 25 24 23 23 24 30 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 3 Reserved for future use. Write as 0 to ensure future compatibility. (bits 3:0 of the trigger are always zero. TRIGGER \$\$ × lk Trigger





PLD OPERATION